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PATENT ABSTRACTS OF JAPAN

(11)Publication number : 11-317887

(43)Date of publication of application : 16.11.1999

(51)Int.Cl. H04N 5/14
G06T 1/00
H04N 5/44

(21)Application number : 10-125053

(22)Date of filing : 07.05.1998

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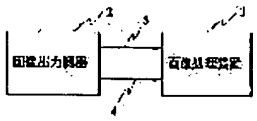
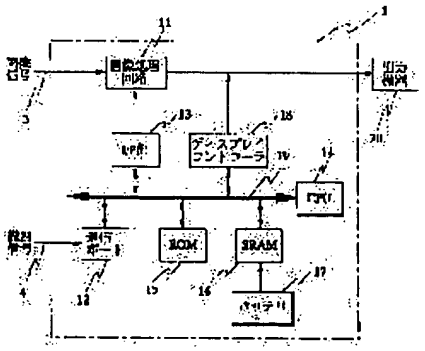
(54) IMAGE PROCESSING UNIT

(57)Abstract:

PROBLEM TO BE SOLVED: To properly and quickly switch an operation mode in response to a connected image output device.

SOLUTION: The image processing unit 1 is provided with an image processing circuit 11 consisting of a field programmable gate array FPGA that receives an image signal from an image output device 2 and applies image processing such as emphasis to the signal, a communication port 12 that receives an identification signal denoting a type of the image output device 2 from the image output device 2, a CPU 14 that applies write control to circuit data to the image processing circuit 11 via an I/F section 13 based on the identification signal received from the communication port 12, a ROM 15 that stores pluralities of circuit data to be written in the image processing circuit 11 and a control program of the CPU 14 in advance, and an SRAM 16 that stores data generated in the case of control by the CPU 14.





LEGAL STATUS

[Date of request for examination] 31.05.2001

[Date of sending the examiner's decision of

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rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

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JAPANESE [JP,11-317887,A]

CLAIMS DETAILED DESCRIPTION TECHNICAL FIELD PRIOR ART EFFECT OF THE INVENTION TECHNICAL PROBLEM MEANS DESCRIPTION OF DRAWINGS DRAWINGS

[Translation done.]

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CLAIMS

[Claim(s)]
[Claim 1] The image processing system characterized by providing the following. A mode storage means to memorize the mode of operation according to the kind of the aforementioned picture output equipment in the image processing system which processes the picture signal inputted from picture output equipment. A mode processing means to process the aforementioned picture signal by setup of the aforementioned mode of operation which the aforementioned mode storage means memorized. A distinction information input means to input the distinction information which distinguishes the kind of the aforementioned picture output equipment. A renewal means of a mode of operation to update the aforementioned mode of operation which compares the aforementioned mode of operation set as the aforementioned mode processing means with the aforementioned mode of operation according to the kind of the aforementioned picture output equipment distinguished using the aforementioned distinction information that the aforementioned distinction information input means inputted, and is memorized by the aforementioned mode storage means based on the comparison result.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to an image processing system and the image processing system which has the feature in the circuit data setting portion of FPGA (Field Programmable Gate Array) in more detail.
[0002]
[Description of the Prior Art] Conventionally, according to the picture output equipment to connect, changing the kind of image processing is performed so that JP,1-26225,B may see in an image processing system, for example. Although there is no indication in the aforementioned example as the method, according to the kind of image processing, changing a path is raised as an easy method.
[0003] For example, as shown in drawing 12 , in the conventional image processing system 101, the picture signal from the picture output equipment which is not illustrated is inputted into plurality 102, 103, and 104, for example, three image-processing circuits, respectively separate processing is performed, and it is outputted to the output equipment 106, such as a monitor, through a selection circuitry 105. Moreover, the recognition signal which shows the kind of picture output equipment (not shown) from the input section of the exterior which is not illustrated is inputted into CPU108 through the communication port 107, and based on this recognition signal, CPU108 is controlling a selection circuitry 105 through the I/F section 109, and choosing one from from among the image-processing circuits 102, 103, and 104, and changes a mode of operation (kind of image processing).
[0004] Moreover, there is an example of the video camera which changes a mode of operation according to a connection place in JP,6-343137,A.
[0005] By the way, LSI called FPGA (Field Programmable Gate Array) has spread recently. The feature of FPGA is that rewriting of circuitry is possible. As for the circuit data of FPGA, it is possible to make it memorize on memory or a medium in the form of binary data. Drawing 13 explains how to change the kind of image processing using FPGA.
[0006] In the image processing system 110 using FPGA, as shown in drawing 13 , the picture signal from the picture output equipment which is not illustrated is inputted into the image-processing circuit 111 which consisted of FPGA, and the processing signal processed by the image-processing circuit 111 is outputted to the output equipment 106, such as a monitor. Although the composition of the image-processing circuit 111 is written in by CPU108, as for the circuit data, plurality is beforehand → circuit configuration
memorized by ROM112. The recognition signal which, on the other hand, shows the kind of picture output equipment (not shown) from the input section of the exterior which is not illustrated is inputted into CPU108 through the communication port 107, and CPU108 chooses circuit data from ROMs112 based on this recognition signal, and writes circuit data in the image-processing circuit 111 through the I/F section 109. According to the kind of picture output equipment, a mode of operation (kind of image processing) can be changed as mentioned above.
[0007]
[Problem(s) to be Solved by the Invention] However, with the above-mentioned image processing

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system 110, although the writing of FPGA requires time, since FPGA was written in after the kind of device was transmitted, when transfer of a kind is overdue by some causes (for example, when powering on of picture output equipment is late etc.), an operator has the problem of waiting still longer time.
[0008] this invention is made in view of the above-mentioned situation, and aims at offering the image processing system which can change the mode of operation according to the picture output equipment connected appropriately and quickly.
[0009]
[Means for Solving the Problem] In the image processing system which processes the picture signal as which the image processing system of this invention was inputted from picture output equipment A mode storage means to memorize the mode of operation according to the kind of the aforementioned picture output equipment, A mode processing means to process the aforementioned picture signal by setup of the aforementioned mode of operation which the aforementioned mode storage means memorized, A distinction information input means to input the distinction information which distinguishes the kind of the aforementioned picture output equipment, Using the aforementioned distinction information that the aforementioned mode of operation and the aforementioned distinction information input means which were set as the aforementioned mode processing means inputted It has a renewal means of a mode of operation to update the aforementioned mode of operation which compares the aforementioned mode of operation according to the kind of the distinguished aforementioned picture output equipment, and is memorized by the aforementioned mode storage means based on the comparison result, and is constituted.
[0010] The aforementioned mode of operation by which the aforementioned renewal means of a mode of operation was set as the aforementioned mode processing means in the image processing system of this invention, By updating the aforementioned mode of operation which compares the aforementioned mode of operation according to the kind of the aforementioned picture output equipment distinguished using the aforementioned distinction information that the aforementioned distinction information input means inputted, and is memorized by the aforementioned mode storage means based on the comparison result It makes it possible to change the mode of operation according to the picture output equipment connected appropriately and quickly.
[0011]
[Embodiments of the Invention] Hereafter, the form of operation of this invention is described, referring to a drawing.
[0012] Drawing in which drawing 1 shows the connection relation between an image processing system and picture output equipment with respect to the form of 1 operation of this invention in drawing 1 or drawing 11 , The block diagram in which drawing 2 shows the composition of the image processing system of drawing 1 , drawing in which drawing 3 shows the memory map of SRAM of drawing 2 , Drawing in which drawing 4 shows the memory map of ROM of drawing 2 , the flow chart which shows the flow of processing according [drawing 5] to CPU of drawing 2 , Explanatory drawing in which drawing 6 explains check processing of the connection device in Step S3 of drawing 5 , Drawing showing an example of a message indicator [in / Step S5 of drawing 5 / in drawing 7], The block diagram in which, as for drawing 8 , circuit data show an example of the image-processing circuit which consisted of FPGA written in and realized by processing of drawing 5 , Explanatory drawing explaining the 1st FIFO circuit where drawing 9 adjusts the delay generated in the 1st block of drawing 8 , and the 2nd block, Explanatory drawing explaining the 2nd FIFO circuit where drawing 10 adjusts the delay generated in the 1st block of drawing 8 and the 2nd block, and drawing 11 are timing charts which show the timing of each signal of the FIFO circuit of drawing 10 .
[0013] While the picture signal outputted from the picture output equipment 2 is inputted through the picture-transmission means 3, between the picture output equipment 2 and image processing systems 1 is connected by means of communications 4, and it has come to be able to perform the uni directional from the picture output equipment 2 to an image processing system 1, or bidirectional communication in the image processing system 1 of the form of this operation, as shown in drawing 1 .
[0014] The image-processing circuit 11 which consisted of FPGA (Field Programmable Gate Array)

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which inputs the picture signal from the picture output equipment 2 through the picture-transmission means 3, and performs image processings, such as emphasis, as an image processing system 1 was shown in drawing 2 , The communication port 12 which inputs the recognition signal which shows the kind of the picture output equipment 2 to picture output equipment 2, CPU14 which performs write-in control of the circuit data to the image-processing circuit 11 through the I/F section 13 based on the inputted recognition signal from the communication port 12, ROM15 which stores beforehand two or more circuit data written in the image-processing circuit 11, and the control program of CPU14, It has the battery 17 which backs up SRAM16 and SRAM16 which store the data generated at the time of control of CPU14, and the display controller 18 who makes an alphabetic data etc. superimpose on the image data processed by the image-processing circuit 11, and is constituted.

[0015] The communication port 12, the I/F section 13, CPU14, ROM15 and SRAM16, and a display controller 18 are connected to a data bus by 19, each circuit is controlled by CPU14, and the image data processed by the image-processing circuit 11 which superimposed the alphabetic data etc. is outputted to the output equipment 20, such as a monitor.

[0016] As shown in drawing 3 , the mode-of-operation data area 21 is formed in the predetermined address position, and as shown in Table 1, the mode-of-operation data corresponding to the connection device are numerically stored in SRAM16 at the mode-of-operation data area 21.

[0017]

[Table 1]

接続機器の種類	動作モードデータ
Aタイプ	1
Bタイプ	2
Cタイプ	3
Dタイプ	4

moreover, two or more kinds of circuit data according to the mode-of-operation data to the image-processing circuit 11 constituted from FPGA by the predetermined address position as shown in ROM15 at drawing 4 other than the control program of CPU14 -- the [the 1st circuit data area 25, the 2nd circuit data area 26, and] -- it is stored in 3 circuit data area 27

[0018] Next, an operation of the form of this operation constituted in this way is explained.

[0019] As shown in drawing 5 , CPU14 reads the mode-of-operation data currently held at Step S1 at SRAM16 after powering on, after initializing fundamental hardware. The circuit data which next read the circuit data corresponding to the mode-of-operation data read at Step S2 from ROM15, and were read to the image-processing circuit 11 which consisted of FPGA are written in. In addition, simultaneously, even if it sets up hardware according to the mode of operation, it can do.

[0020] And picture output equipment 2 actually connected is checked at Step S3. A check is performed by the means of communications 4 through the communication port 12, for example, RS-232C is known. The procedure of a check of a connection device is shown in drawing 6 . First, "device type inquiry command" 31 are transmitted to the picture output equipment 2 from an image processing system 1. According to it, "notice of device type" 32 are transmitted to an image processing system 1 from the picture output equipment 2.

[0021] In addition, an image processing system 1 is able to always transmit a device type to an image processing system 1 from the picture output equipment 2, and to receive suitably. In this case, means of communications 4 can be managed with one-way communication.

[0022] Next, in step S4, the mode-of-operation data corresponding to the picture output equipment 2 obtained as mentioned above are compared with the mode-of-operation data saved at SRAM16. Since the image-processing circuit 11 according to the picture output equipment 2 is written in when both are in agreement, it ends as it is. When it differs, it progresses to Step S5.

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[0023] At Step S5, the mode-of-operation data corresponding to the picture output equipment 2 actually connected are saved at SRAM16. And at Step S6, as shown in drawing 7 , a message 36 is superimposed on the processing picture 35 of the image-processing circuit 11 by the display controller 18, an operator is told about the right circuit data not having been written in the image-processing circuit 11, and processing is ended.
[0024] Here, according to this message 36, an operator once turns off the picture output equipment 2, and considers the case where it reputs in.
[0025] An image processing system 1 performs the procedure of the flow chart of drawing 5 again. Step S1 to the step S3 is the same as that of the time of the above-mentioned starting. In step S4, it is saved at SRAM16 and mode-of-operation data and the mode-of-operation data corresponding to the picture output equipment 2 actually connected are in agreement. It is because the mode of operation corresponding to the picture output equipment 2 which is Step S5 and is actually connected last time at the time of starting is saved at SRAM16.
[0026] Next, operation of the image-processing circuit 11 which consisted of FPGA to which the writing of circuit data was performed by control of CPU14 is described.
[0027] the image-processing circuit 11 created with circuit data as shown in drawing 8 -- for example, different processing to the inputted picture signal is performed -- the 1st block consists of 41 and composition block 43 which compounds with 42 the 2nd block of the 1st block of 41 and the picture processed by 42 [block / 2nd]
[0028] And in the image-processing circuit 11, as for the inputted picture, the 1st block of 41 and processing which was inputted into 42 the 2nd block and is different, respectively are performed. Each output is inputted into the synthetic block 43, and is compounded and outputted to one picture.
[0029] here -- for example, 41 is full color the 1st block -- outputting a 24-bit processing result, 42 outputs the 2nd block of the 1-bit information on whether the processed picture is displayed and the so-called mask information
[0030] If the 2nd block of the 1st block of a difference is in delay by 42 with 41 at this time, a gap of the position of a picture will be produced. Therefore, it is necessary to adjust delay of either or both. Then, FIFO (First In FirstOut= FIFO) memory is used for adjustment of delay.
[0031] Although FIFO memory can be delayed arbitrarily, the maximum of the size of a picture is restricted within the limits of capacity. Temporarily, when the picture of 640 dot x480 line is delayed, 640x480=307,200 dot capacity is required. When the capacity of memory is smaller than this, more than one are used and capacity is extended.
[0032] Although capacity will be extended using memory two or more when the capacity of memory is smaller than this For example, two to which both the input and the output are connected in parallel in the FIFO circuit 50 as shown in drawing 9 For example, capacity extends capacity using the FIFO memory 51 and 52 of 262,144 dots (<307,200 dot) by inputting 1 dot of data into this two FIFO memory 51 and 52 at a time by turns, and performing an output by turns.

reconfigure memory

[0033] By the way, FIFO memory has the data width of face of I/O, and the thing of 8-bit width of face is circulating widely. However, in actual application, there is also thing sufficient for 1-bit information like the mask signal of the above-mentioned picture. When such and the data of 1-bit width of face are delayed using the FIFO memory of the 8-bit width of face shown in drawing 9 , 7 bits of FIFO memory always are not used, but it becomes useless.
[0034] Then, when such, how to extend capacity is described, without using two or more FIFO memory.

[0035] As shown in drawing 10 , the FIFO circuit 60 of the 1-bit width of face which realized capacity extension consists of a shift register 61, FIFO memory 62, and a selector 63, and with reference to the timing chart of drawing 11 , the signal inputted from Din is sent to a shift register 61, is changed into 2 bits from 1 bit with this shift register 61 synchronizing with the pixel clock phi 1, and is inputted into the FIFO memory 62.
[0036] The clock phi 2 of 2 dividing of the pixel clock phi 1 is supplied to the FIFO memory 63, and the data from a shift register 61 are incorporated by the FIFO memory 62 to the timing of rising edge ** of a

(9)

clock phi 2. The amount of delay of the FIFO memory 62 is determined by the time difference of the pulse of both light reset and lead reset, and the data inputted into the shift register 61 are outputted to the inputs D1 and D2 of the FIFO memory 62 after a fixed time delay.
[0037] The outputs Q1 and Q2 of the FIFO memory 62 are selectors 63, are again returned to 1 bit from 2 bits, and are outputted from a selector 63. In addition, a selector 63 may consist of shift registers.
[0038] Thus, in the image processing system 1 of the form of this operation, since picture output equipment 2 of a connection place is performed after writing the circuit data beforehand stored in SRAM16 in FPGA which constitutes the image-processing circuit 11, an image processing system 1 can be started, without waiting for the check of the picture output equipment 2. That is, since an image processing system 1 can be started first and picture output equipment 2 of a connection place is performed for example, next even when powering on of the picture output equipment 2 of a connection place is late, an operator does not need to wait long time.
[0039] moreover, when the kinds of the kind of circuit data and the picture output equipment 2 which were written in FPGA which constitutes the image-processing circuit 11 differ While reading the circuit data corresponding to the picture output equipment 2 of a connection place from ROM15 and storing in SRAM16 Since re-starting of the picture output equipment 2 of a connection place is directed by the message, an operator can start an image processing system 1 certainly and easily by re-starting picture output equipment 2 according to this message.
[0040] [Additional remark]
(Additional remark term 1) In the image processing system which processes the picture signal inputted from picture output equipment By setup of the aforementioned mode of operation which a mode storage means to memorize the mode of operation according to the kind of the aforementioned picture output equipment, and the aforementioned mode storage means memorized A mode processing means to process the aforementioned picture signal, and a distinction information input means to input the distinction information which distinguishes the kind of the aforementioned picture output equipment, The aforementioned mode of operation set as the aforementioned mode processing means is compared with the aforementioned mode of operation according to the kind of the aforementioned picture output equipment distinguished using the aforementioned distinction information that the aforementioned distinction information input means inputted. The image processing system characterized by having a renewal means of a mode of operation to update the aforementioned mode of operation memorized by the aforementioned mode storage means based on the comparison result.
[0041] (Additional remark term 2) The aforementioned mode processing means is an image processing system given in the additional remark term 1 characterized by being FPGA (Field Programmable Gate Array).
[0042] (Additional remark term 3) In the image-processing method of processing the picture signal inputted from picture output equipment The mode setting process which sets up the mode of operation according to the kind of the aforementioned picture output equipment for processing the aforementioned picture signal memorized by the mode storage means, The device distinction process which distinguishes the kind of the aforementioned picture output equipment, and the aforementioned mode of operation set up by account mode down stream processing, The image-processing method characterized by having the renewal process of a mode of operation which updates the aforementioned mode of operation which compares the aforementioned mode of operation according to the kind of the aforementioned picture output equipment distinguished according to the aforementioned device distinction process, and is memorized by the aforementioned mode storage means based on the comparison result.
[0043]
[Effect of the Invention] The mode of operation by which the renewal means of a mode of operation was set as the mode processing means according to the image processing system of this invention as explained above, Since the aforementioned mode of operation which compares the mode of operation according to the kind of picture output equipment distinguished using the distinction information which the distinction information input means inputted, and is memorized by the aforementioned mode storage

means based on the comparison result is updated It is effective in the ability to change the mode of operation according to the picture output equipment connected appropriately and quickly.

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DRAWINGS

[Drawing 1] picture output equipment (monitor)

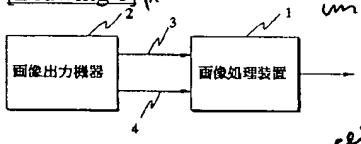
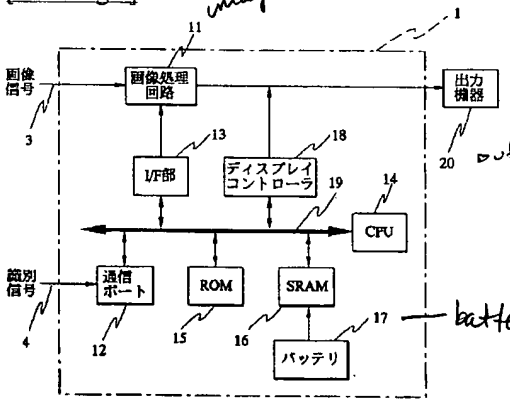


image processing system

image processing circuit

[Drawing 2]



ROM 15: stores circuit data

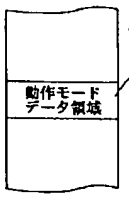
output equipment (monitor)

18: display controller

19: data bus

battery

[Drawing 3]

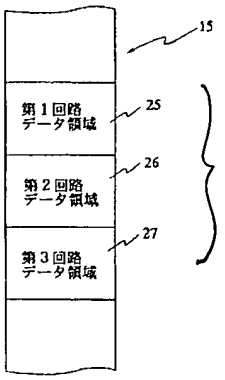


SRAM

mode of operation data

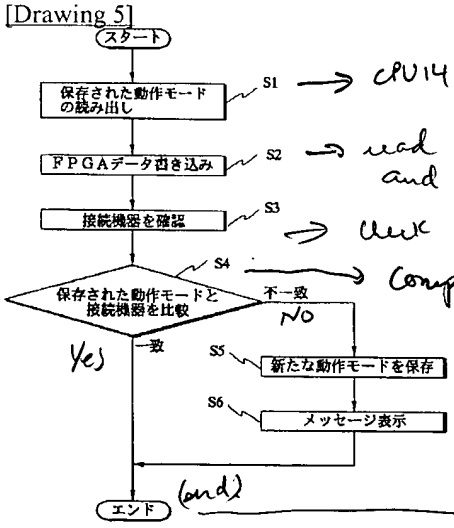
[Drawing 4]

(12)



Circuit data stored at address locations (1, 2, 3) in ROM 15

[Drawing 5]



S1 → CPU 14 reads mode of operations data from SRAM 16

S2 → read circuit data (from ROM 15) corresponding to mode of operations data and supply this circuit data to image processing circuit 11

S3 → check connection between output equipment 2 & system 1

S4 → Compare data from S1, S2.

NO

Yes

S5 updated.

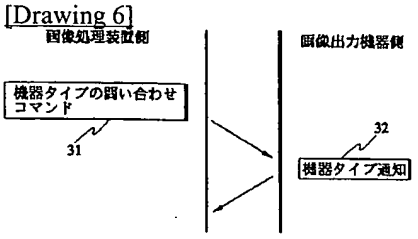
S6 messages → indicate no written to 11

(end)

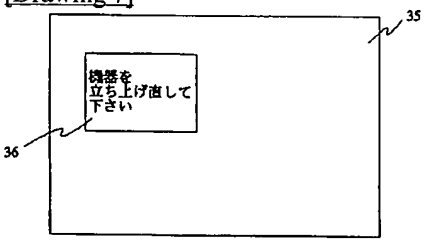
when S4 is Yes, circuit 11 according to equipment 2 is written.

S4 is NO, goto S5

[Drawing 6]



[Drawing 7]

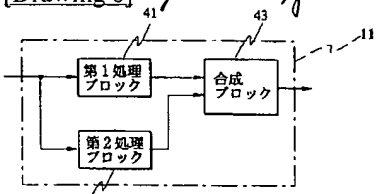


full color processing block to produce 24-bit output.

Synthetic block

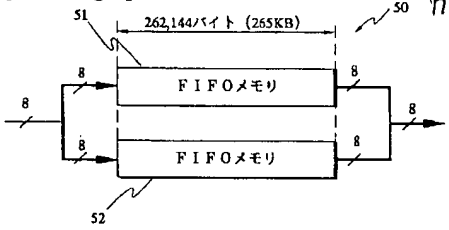
(13)

[Drawing 8]



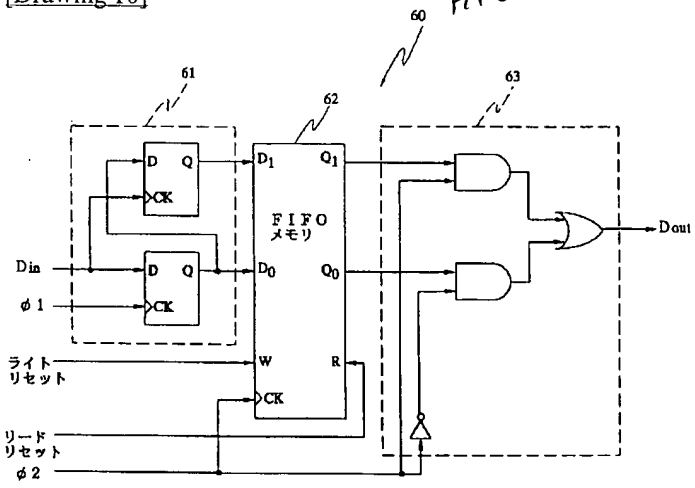
output 1-bit informations (mask info)

[Drawing 9]



FIFO circuit

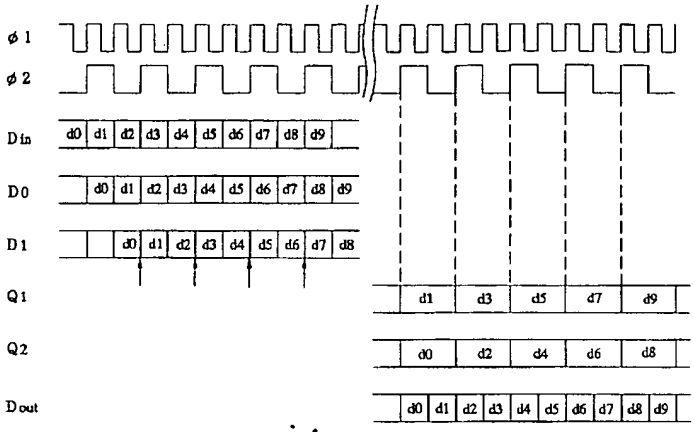
[Drawing 10]



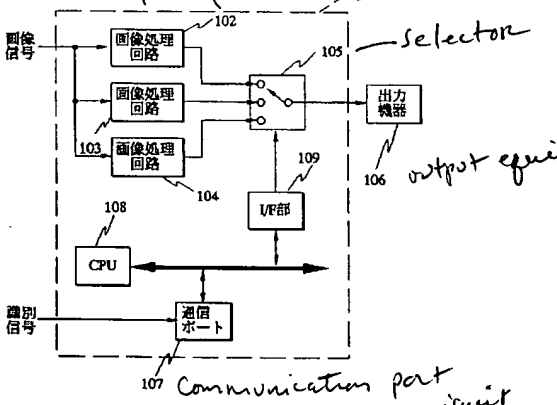
FIFO circuit

[Drawing 11]

(14)

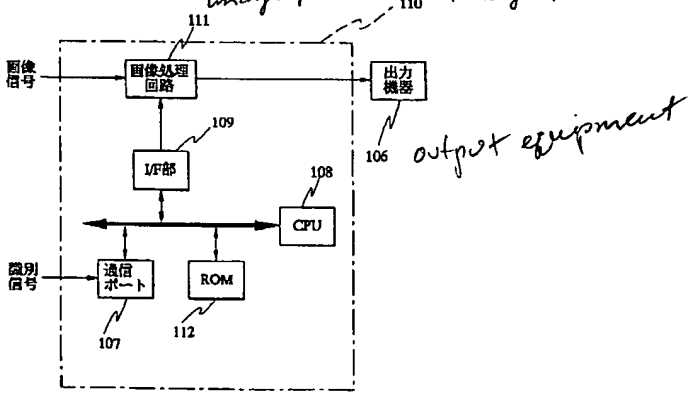


[Drawing 12]



102, 103, 104 + image processing circuits

[Drawing 13]



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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Drawing showing the connection relation between the image processing system concerning the gestalt of 1 operation of this invention, and picture output equipment
[Drawing 2] The block diagram showing the composition of the image processing system of drawing 1
[Drawing 3] Drawing showing the memory map of SRAM of drawing 2
[Drawing 4] Drawing showing the memory map of ROM of drawing 2
[Drawing 5] The flow chart which shows the flow of processing by CPU of drawing 2
[Drawing 6] Explanatory drawing explaining check processing of the connection device in Step S3 of drawing 5
[Drawing 7] Drawing showing an example of the message indicator in Step S5 of drawing 5
[Drawing 8] The block diagram showing an example of the image-processing circuit which consisted of FPGA which circuit data are written in by processing of drawing 5 and realized
[Drawing 9] Explanatory drawing explaining the 1st FIFO circuit which adjusts the delay generated in the 1st block of drawing 8 , and the 2nd block
[Drawing 10] Explanatory drawing explaining the 2nd FIFO circuit which adjusts the delay generated in the 1st block of drawing 8 , and the 2nd block
[Drawing 11] The timing chart which shows the timing of each signal of the FIFO circuit of drawing 10
[Drawing 12] The block diagram showing the 1st example of composition of the conventional image processing system
[Drawing 13] The block diagram showing the 2nd example of composition of the conventional image processing system
[Description of Notations]
1 -- Image processing system
2 -- Picture output equipment
11 -- Image-processing circuit
12 -- Communication port
13 -- I/F section
14 -- CPU
15 -- ROM
16 -- SRAM
17 -- Battery
18 -- Display controller
19 -- Data bus
20 -- Output equipment

[Translation done.]